US03 0199 WD

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APPLICATION NUMBER: *60/482,278*
FILING DATE: *June 25, 2003*

REC'D - 6 AUG 2004
WIPO PCT

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06/25/03

PTO/SB/16 (02-01)
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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53 (c).

Express Mail Label No. EV 312 069 882 | Date of Deposit: JUNE 25, 2003

INVENTOR(S)

Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
JOSEPH M.	AMATO	BEACON, NY

☐ Additional inventors are being named on the ____ separately numbered sheets attached hereto

01008 U.S. PTO
60/482278
06/25/03

TITLE OF THE INVENTION (280 characters max)

"OFFSET DEPENDENT RESISTOR FOR MEASURING MISALIGNMENT OF STITCHED MASKS"

CORRESPONDENCE ADDRESS

Direct all correspondence to:

☒ Customer Number 24737 → *24737*

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ENCLOSED APPLICATION PARTS (check all that apply)

☒ Specification Number of Pages 23 ☐ CD(s), Number

X Drawing(s) Number of Sheets 3 X Other (specify) IDS

☐ Application Data Sheet. See 37 CFR 1.76

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT (check one)

☐ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check or money order is enclosed to cover the filing fees

FILING FEE AMOUNT ($)

☒ The Commissioner is hereby authorized to charge filing fees or credit any overpayment to Deposit Account Number: 14-1270 160.00

☐ Payment by credit card. Form PTO-2038 is attached.

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☒ No.

☐ Yes, the name of the U.S. Government agency and the Government contract number are: ____.

Respectfully submitted,

SIGNATURE _____ Date: JUNE 25, 2003

TYPED or PRINTED NAME STEVEN R. BIREN REGISTRATION NO.: 26,531 (if appropriate)

TELEPHONE (914) 333-9630 Docket Number: US030199

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

This collection of information is required by 37 CFR 1.51. The information is used by the public to file (and by the PTO to process) a provisional application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the complete provisional application to the PTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C., 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Box Provisional Application, Assistant Commissioner for Patents, Alexandria, VA 22313.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of JOSEPH M. AMATO

17648 U.S. PTO
06/25/03

Atty. Docket US 030199

Serial No.:

Filed: CONCURRENTLY

Title: OFFSET DEPENDENT RESISTOR FOR MEASURING MISALIGNMENT OF STITCHED MASKS

Commissioner for Patents
Alexandria, VA 22313

AUTHORIZATION PURSUANT TO 37 CFR .1.136(a)(3) AND TO CHARGE DEPOSIT ACCOUNT

Sir:

The Commissioner is hereby requested and authorized to treat any concurrent or future reply in this application requiring a petition for extension of time for its timely submission, as incorporating a petition for extension of time for the appropriate length of time.

Please charge any additional fees which may now or in the future be required in this application, including extension of time fees, but excluding the issue fee unless explicitly requested to do so, and credit any overpayment, to Deposit Account No. 14-1270.

Respectfully submitted,

By
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OFFSET DEPENDENT RESISTOR FOR MEASURING MISALIGNMENT OF STITCHED MASKS

The present invention relates to measuring misalignment of stitched masks in a semiconductor manufacturing process, and more specifically relates to a sensitivity enhanced matched offset dependent resistor structure for electrically measuring unidirectional misalignment of stitched masks for etched interconnect layers.

Most semiconductor devices are built using a number of material layers. Each layer is patterned to add or remove selected portions to form circuit features that will eventually make a complete integrated circuit. The patterning process, known as photolithography, defines the dimensions of the circuit features using masks that selectively block a light source.

As the complexity of integrated circuits increases, the number and size of circuits become larger and larger, often consuming an entire wafer. In Wafer Scale Integration (WSI), the retical of a standard mask is often too small to expose the entire wafer. In these cases, multiple masks must be used for a single layer in fabrication. Specifically, circuits created by a first mask are "stitched" together with circuits created by a second mask in an overlapping region.

Misalignments in the stitching can cause detrimental effects, and it is therefore desirable to know when they occur.

Present methods for identifying misalignments include using a scanning microscope to study the device. This methodology is both time-consuming and costly, as the device must be etched to expose the stitched area, and then carefully studied to identify any misalignment. Accordingly, a need exists for a simplified process for identifying misalignments in stitched circuits.

The present invention addresses the above-mentioned problems, as well as others, by providing a set of offset dependant resistor structures formed in part by each of a reference mask and secondary mask. The resistor values will vary from an ideal value when an offset occurs and be equal to the ideal value when no offset exists. Detection is isolated to a single axis for each resistor structure, and the structure can be repeated in a compact design to offer ease of use and increased sensitivity to misalignment.

In a first aspect, the invention provides a method for identifying misalignments in an overlapping region of a stitched circuit in an integrated circuit fabrication process, comprising: creating a first circuit using a reference mask, wherein the first circuit includes a first part of an offset dependent resistor structure in the

overlapping region; creating a second circuit using a secondary mask, wherein the second circuit includes a second part of the offset dependent resistor structure in the overlapping region, wherein the offset dependent resistor structure includes a plurality of nubs that interconnect the first part and the second part of the offset dependent resistor structure; measuring a resistance across the offset dependent resistor structure; and determining an amount of misalignment based on the measured resistance.

In a second aspect, the invention provides an offset dependent resistor structure for identifying a misalignment in an overlapping region of a stitched portion of an integrated circuit, comprising: a first part of an offset dependent resistor structure created in the overlapping region using a reference mask; a second part of the offset dependent resistor structure superimposed on the first part in the overlapping region using a secondary mask; and a plurality of nubs that interconnect the first part and the second part of the offset dependent resistor structure to form a single electrical pathway, wherein the resistance of the single electrical pathway is dependent upon the length of the nubs that interconnect the first part and the second part of the offset dependent resistor structure.

In a third aspect, the invention provides a system for measuring misalignments in an overlapping region of a

stitched portion of an integrated circuit, comprising: an offset dependent resistor structure, including: a first part created in the overlapping region using a reference mask, a second part superimposed on the first part in the overlapping region and created using a secondary mask, and a plurality of nubs oriented in a first uniform direction that interconnect the first part and the second part to form a single electrical pathway, wherein the resistance of the single electrical pathway is dependent upon the length of the nubs that interconnect the first part and the second part; and a system for measuring the resistance across the single electrical pathway.

In a fourth aspect, the invention provides a method for identifying misalignments in an overlapping region of a stitched circuit in a integrated circuit fabrication process, comprising: creating a first circuit using a reference mask, wherein first circuit includes in the overlapping region a first part of a first offset dependent resistor structure and a first part of a second offset dependent resistor structure; creating a second circuit using a secondary mask, wherein the second circuit includes in the overlapping region a second part of the first offset dependent resistor structure and a second part of the second offset dependent resistor structure, wherein the first offset dependent resistor structure includes a plurality of first nubs that

interconnect the first part and the second part of the first offset dependent resistor structure, wherein the second offset dependent resistor structure includes a plurality of second nubs that interconnect the first part and the second part of the second offset dependent resistor structure, and wherein the first and second nubs are oriented in a uniform direction; measuring a resistance across both the first and second offset dependent resistor structures; and determining an amount of misalignment based on the measured resistances.

These and other features of this invention will be more readily understood from the following detailed description of the various aspects of the invention taken in conjunction with the accompanying drawings in which:

Figure 1 depicts an overlapping region of an integrated circuit chip in accordance with the present invention.

Figure 2A depicts a first portion of an offset dependant resistor structure created by a first mask in accordance with the present invention.

Figure 2B depicts a second portion of the offset dependant resistor structure created by a second mask in accordance with the present invention.

Figure 3 depicts first and second portions of Figures 2A and 2B superimposed with no offset.

Figure 4 depicts first and second portions of Figures 2A and 2B superimposed with a positive offset.

Figure 5 depicts first and second portions of Figures 2A and 2B superimposed with a negative offset.

Figure 6A depicts a first portion of a second offset dependant resistor structure created by a first mask in accordance with the present invention.

Figure 6B depicts a second portion of the second offset dependant resistor structure created by a second mask in accordance with the present invention.

Figure 7 depicts first and second portions of Figures 6A and 6B superimposed with no offset.

Figure 8 depicts first and second portions of Figures 6A and 6B superimposed with a positive offset.

Figure 9 depicts first and second portions of Figures 6A and 6B superimposed with a negative offset.

Referring now to the drawings, Figure 1 depicts a portion of an overlapping region 10 of an integrated circuit chip. In the overlapping region 10, a first set of circuit features may be created using a reference mask, and a second set of circuit features may be created using a secondary mask (not shown). Accordingly, some of the circuit features of both must be "stitched" together to integrate the circuits laid down by the reference mask and the secondary mask. In

this exemplary embodiment, four offset dependant resistor structures 12a, 12b, 14a and 14b are utilized to determine any misalignment between the circuits.

Structures 12a and 12b are implemented using a first embodiment (described in more detail below with regard to Figures 2-5) that includes a first part 24 created by the primary mask and a second part 26 created by a secondary mask. Structures 12a and 12b provide an increased resistance when the second part 26 is misaligned towards the first part 24 (i.e., a positive misalignment as shown by the directional arrows).

Structures 14a and 14b are implemented using a second embodiment (described in more detail below with regard to Figures 6-9) that includes a first part 20 created by the primary mask and a second part 22 created by a secondary mask. Structures 14a and 14b provide an increased resistance when the second part 22 is misaligned away the first part 20 (i.e., a negative misalignment as shown by the directional arrows).

Accordingly, structures 12a and 14a measure misalignment in the up-down directions, while structures 12b and 14b measure misalignment in the left-right direction. It should be understood that while the exemplary embodiment of Figure 1 depicts the use of four offset dependant resistor structures, the invention could be implemented using as few as one

structure or as many as desired. Each of the structures 12a, 12b, 14a and 14b include test pads 28, 30 (or any other connection structure) for measuring the resistance. In one exemplary embodiment, a test system 11 may be utilized with probes 13 to measure the resistance, compare it to an ideal value representative of a zero misalignment, and calculate a misalignment. In an alternative embodiment, the structures 12a, 12b, 14a and 14b could be connected to on-board circuitry, which could capture and report the resistance value and/or amount of misalignment, e.g., using an operational amplifier.

Referring now to Figures 2A, 2B and 3-5, a further description of the first type of offset dependant resistor structure 12 (i.e., 12a and 12b of Figure 1) is shown. Figure 2A depicts the first part 24 of structure 12 created by a reference mask and Figure 2B depicts the second part 26 of the structure 12 created by a secondary mask. First part 24 includes a pair of open rectangular substructures 32, each having two interface points 34. First part also includes a pair of test pads 28 and 30. Second part 26 includes three substructures 36, 38 and 40 that have four interface nubs 42.

Figures 3-5 depict three cases of offset dependent resistor structure 12 having the second part 26 superimposed on the first part 24. As can be seen, when the substructures of both parts are laid down, a single electrical pathway is

created between the test pads. The structure includes four nubs 42 that interface the two parts. Because of the design of the substructures, an up or down misalignment or offset will require more or less of each nub 42 to be used, resulting in either a longer or shorter electrical pathway. As is generally known, the longer the pathway, the greater the resistance. Accordingly, by measuring the resistance through the pathway, a relative amount of vertical misalignment can be ascertained.

More specifically, a relative increase in resistance occurs when the second part 26 is misaligned toward the first part 24 (positive misalignment), and a relative decrease in resistance occurs when the second part 26 is misaligned away from the first part 24 (negative misalignment). The case depicted in Figure 3 depicts the ideal case where no misalignment occurs. That is, the exposed length of the interface nubs 42 between the substructures 34 of the first part and the substructures 36, 38 and 42 of the second part matches an "ideal" length.

Figure 4 depicts the case where the second part 26 is misaligned upward and to the right of the first part 26. As can be seen, the exposed length of the nubs 24 has increased relative to the ideal length of Figure 3. In this case, the electrical pathway is longer, and therefore structure 12 in

Figure 4 will have a greater resistance than structure 12 of Figure 3.

Figure 5 depicts the case where the second part 26 is misaligned downward and to the left of the first part 26. As can be seen, the exposed length of the nubs 24 has decreased relative to the ideal length of Figure 3. In this case, the electrical pathway is shorter, and therefore the structure 12 in Figure 4 will have less resistance than the structure of Figure 3.

Increased sensitivity is achieved by providing an offset resistor structure that includes a plurality of interface nubs 42 along the pathway. In this embodiment, four nubs 42 are utilized, with each of the nubs 42 adding or reducing the overall length of the pathway when a vertical misalignment occurs. Thus, the sensitivity of the structure is increased by a factor of four. It should be understood that the structure 12 measures misalignment in a single direction (e.g., vertical). To identify a misalignment in a second direction (e.g., horizontal) a second structure 12 may be used, except that it must be oriented in the desired direction, e.g., perpendicularly to the first, as shown in Figure 1 (see, 12a vs. 12b).

Figures 6-9 depict a second implementation of an offset dependent resistor structure 14 (i.e., structures 14a and 14b of Figure 1). In this embodiment, a first part 20 created by

a reference mask is shown in Figure 6A and includes a pair of test pads and three substructures 44, 46 and 48. A second part 22 created by a secondary mask includes a pair of E-shaped substructures 50. Each E-shaped substructure 50 includes a pair of nubs 52. Figures 7-9 depict three cases in which the second part 22 has been superimposed on the first part 20. Figure 7 depicts the zero offset case where the exposed portion of each nub 52 is an ideal length. Figure 8 depicts the case where the second part 22 is misaligned upward and to the right relative to the first part 20. In this case, the exposed portion of each nub 52 is smaller relative to the ideal case, thereby creating a relatively lower resistance. Figure 9 depicts the case where the second part 22 is misaligned downward and to the left relative to the first part 20. In this case, the exposed portion of each nub 52 is larger relative to the ideal case, thereby creating a relatively greater resistance.

Similar to offset dependent resistor structure 12, offset dependent resistor structure 14 includes four nubs to provide increased sensitivity. However, structure 14 shown in Figures 6-9 differs from the offset dependent resistor structure 12 shown in Figures 2-5 in that structure 14 generates a relatively lower resistance when the second part 22 is misaligned towards the first part 20 (positive misalignment), and generates a relatively higher resistance

when the second part 22 is misaligned away from the first part 20 (negative misalignment).

Note however that in the ideal cases shown in Figures 3 and 7, structures 12 and 14 are electrically equivalent, i.e., they have the same resistive values. In particular, both ideal structures have the same number of turns and the same overall pathway length. Thus, when a positive offset occurs, the resistance value of structure 12 will increase by the same amount as the resistive value of structure 14 will decrease. Obviously, the overall arrangement of the substructures can be altered to produce similar results, and such alterations fall within the scope of this invention.

The foregoing description of the preferred embodiments of the invention has been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously many modifications and variations are possible in light of the above teachings. Such modifications and variations that are apparent to a person skilled in the art are intended to be included within the scope of this invention as defined by the accompanying claims.

CLAIMS

1. A method for identifying misalignments in an overlapping region of a stitched circuit in an integrated circuit fabrication process, comprising:

creating a first circuit using a reference mask, wherein first circuit includes a first part of an offset dependent resistor structure in the overlapping region;

creating a second circuit using a secondary mask, wherein the second circuit includes a second part of the offset dependent resistor structure in the overlapping region, wherein the offset dependent resistor structure includes a plurality of nubs that interconnect the first part and the second part of the offset dependent resistor structure;

measuring a resistance across the offset dependent resistor structure; and

determining an amount of misalignment based on the measured resistance.

2. The method of claim 1, wherein:

one of the parts of the offset dependent resistor structure comprises a pair of open rectangular substructures, each having two open terminal points; and

the other part of the offset dependent resistor structure comprises three substructures that interconnect

with the open terminal points of the rectangular substructures to form a single electrical pathway when the first and second parts are superimposed.

3. The method of claim 2, wherein one of the parts of the offset dependent resistor structure structure comprises a pair of test pads.

4. The method of claim 2, wherein the first part and the second part of the offset dependent resistor structure interconnect via four nubs, wherein each nub is oriented in a uniform direction.

5. The method of claim 4, wherein:

a zero misalignment in the uniform direction results in each nub having a first length;

a positive misalignment in the uniform direction results in each nub having a second length that is greater than the first length; and

a negative misalignment in the uniform direction results in each nub having a third length that is less than the first length.

6. The method of claim 5, wherein:

zero misalignment results in a first resistive value along the single electrical pathway;

positive misalignment results in a second resistive value along the single electrical pathway that is greater than the first resistive value; and

negative misalignment results in a third resistive value along the single electrical pathway that is less than the first resistive value.

7. The method of claim 6, wherein the step of determining the amount of misalignment based on the measured resistance includes the step of comparing the measured resistance to a known resistance value representative of the case of zero misalignment.

8. The method of claim 1, wherein:

one of the parts of the offset dependent resistor structure comprises a pair of open E-shaped substructures, each having two open terminal points; and

the other part of the offset dependent resistor structure comprises three substructures that interconnect with the open terminal points of the E-shaped substructures to form a single electrical pathway when the two parts are superimposed.

9. The method of claim 8, wherein one of the parts of the offset dependent resistor structure comprises a pair of test pads.

10. The method of claim 8, wherein the first part and the second part of the offset dependent resistor structure interconnect via four nubs, wherein each nub is oriented in a uniform direction.

11. The method of claim 10, wherein:

a zero misalignment in the uniform direction results in each nub having a first length;

a positive misalignment in the uniform direction results in each nub having a second length that is less than the first length; and

a negative misalignment in the uniform direction results in each nub having a third length that is greater than the first length.

12. The method of claim 11, wherein:

zero misalignment results in a first resistive value along the single electrical pathway;

positive misalignment results in a second resistive value along the single electrical pathway that is less than the first resistive value; and

negative misalignment results in a third resistive value along the single electrical pathway that is greater than the first resistive value.

13. The method of claim 12, wherein the step of determining the amount of misalignment based on the measured resistance includes the step of comparing the measured resistance to a known resistance value determined for the case of zero misalignment.

14. An offset dependent resistor structure for identifying a misalignment in an overlapping region of a stitched portion of an integrated circuit, comprising:

a first part of an offset dependent resistor structure created in the overlapping region using a reference mask;

a second part of the offset dependent resistor structure superimposed on the first part in the overlapping region using a secondary mask; and

a plurality of nubs that interconnect the first part and the second part of the offset dependent resistor structure to form a single electrical pathway, wherein the resistance of the single electrical pathway is dependent upon the length of the nubs that interconnect the first part and the second part of the offset dependent resistor structure.

15. The offset dependent resistor structure of claim 14, further comprising a pair of test pads at ends of the single electrical pathway.

16. The offset dependent resistor structure of claim 14, wherein:

the first part of the offset dependent resistor structure comprises a pair of open rectangular substructures, each having two open terminal points; and

the second part of the offset dependent resistor structure comprises three substructures that interconnect with the open terminal points of the open rectangular substructures to form the single electrical pathway.

17. The offset dependent resistor structure of claim 14, wherein:

the first part of the offset dependent resistor structure comprises a pair of open E-shaped substructures, each having two open terminal points; and

the second part of the offset dependent resistor structure comprises three substructures that interconnect with the open terminal points of the E-shaped substructures to form a single electrical pathway.

18. The offset dependent resistor structure of claim 14, wherein the first part and the second part of the offset

dependent resistor structure interconnect via four nubs, wherein each nub is oriented in a uniform direction.

19. A system for measuring misalignments in an overlapping region of a stitched portion of an integrated circuit, comprising:

an offset dependent resistor structure, including:

a first part created in the overlapping region using a reference mask,

a second part superimposed on the first part in the overlapping region and created using a secondary mask; and

a plurality of nubs oriented in a first uniform direction that interconnect the first part and the second part to form a single electrical pathway,, wherein the resistance of the single electrical pathway is dependent upon the length of the nubs that interconnect the first part and the second part, and

a system for measuring the resistance across the single electrical pathway.

20. The system of claim 19, wherein the system for measuring the resistance comprises a pair of test pads at the ends of the single electrical pathway and a pair of probes.

21. The system of claim 19, further comprising a second offset dependent resistor structure, including:

a first part created in the overlapping region using a reference mask,

a second part created in the overlapping region using a secondary mask, and

a plurality of second nubs oriented in a second uniform direction that interconnect the first part and the second part to form a single electrical pathway, wherein the second uniform direction is perpendicular to the first uniform direction.

22. A method for identifying misalignments in an overlapping region of a stitched circuit in a integrated circuit fabrication process, comprising:

creating a first circuit using a reference mask, wherein first circuit includes in the overlapping region a first part of a first offset dependent resistor structure and a first part of a second offset dependent resistor structure;

creating a second circuit using a secondary mask, wherein the second circuit includes in the overlapping region a second part of the first offset dependent resistor structure and a second part of the second offset dependent resistor structure, wherein the first offset dependent resistor structure includes a plurality of first nubs that interconnect the first part and the second part of the first

offset dependent resistor structure, wherein the second offset dependent resistor structure includes a plurality of second nubs that interconnect the first part and the second part of the second offset dependent resistor structure, and wherein the first and second nubs are oriented in a uniform direction;

measuring a resistance across both the first and second offset dependent resistor structures; and

determining an amount of misalignment based on the measured resistances.

23. The method of claim 22, wherein:

a zero misalignment in the uniform direction results in all of the first nubs and second nubs being substantially equal to a first length; and

a non-zero misalignment in the uniform direction results in the first nubs having a length less than the first length and the second nubs having a length greater than the first length.

24. The method of claim 22, wherein a zero misalignment in the uniform direction results in the first and second offset dependent resistor structures having the same resistive values.

25. The method of claim 22, wherein a non-zero misalignment in the uniform direction results in the second offset

dependent resistor structure having a resistive value that is substantially the negative of the resistive value of the first offset dependent resistor structure.

ABSTRACT

A system and method for identifying misalignments in an overlapping region of a stitched circuit in an integrated circuit fabrication process. The method comprises: creating a first circuit using a reference mask, wherein first circuit includes a first part of an offset dependent resistor structure in the overlapping region; creating a second circuit using a secondary mask, wherein the second circuit includes a second part of the offset dependent resistor structure in the overlapping region, wherein the offset dependent resistor structure includes a plurality of nubs that interconnect the first part and the second part of the offset dependent resistor structure; measuring a resistance across the offset dependent resistor structure; and determining an amount of misalignment based on the measured resistance.

PTO/SB/01 (03-01)
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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☒ Declaration Submitted With Initial Filing OR ☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	PHUS030199WO
First Named Inventor	JOSEPH M. AMATO
COMPLETE IF KNOWN	
Application Number	/
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

"OFFSET DEPENDENT RESISTOR FOR MEASURING MISALIGNMENT OF STITCHED MASKS"

(Title of the Invention)

the specification of which

☒ is attached hereto

OR

☐ was filed on (MM/DD/YYYY) ☐ as United States Application Number or PCT International Application Number ☐ and was amended on (MM/DD/YYYY) ☐ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY) Country	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
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☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

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DECLARATION — Utility or Design Patent Application

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NAME OF SOLE OR FIRST INVENTOR: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any]) JOSEPH M.		Family Name or Surname AMATO	
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NAME OF SECOND INVENTOR: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
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☐ Additional Inventors are being named on the ____ supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of | Atty. Docket

JOSEPH M. AMATO | US 030199

Serial No.:

Filed: CONCURRENTLY

Title: OFFSET DEPENDENT RESISTOR FOR MEASURING MISALIGNMENT OF STITCHED MASKS

Commissioner for Patents
Alexandria, VA 22313

APPOINTMENT OF ASSOCIATES

Sir:

The undersigned Attorney of Record hereby revokes all prior appointments (if any) of Associate Attorney(s) or Agent(s) in the above-captioned case and appoints:

STEVEN R. BIREN **(Registration No. 26,531)**

c/o U.S. PHILIPS CORPORATION, Intellectual Property Department, P.O. BOX 3001, Briarcliff Manor, New York 10510, his Associate Attorney(s)/Agent(s) with all the usual powers to prosecute the above-identified application and any division or continuation thereof, to make alterations and amendments therein, and to transact all business in the Patent and Trademark Office connected therewith.

ALL CORRESPONDENCE CONCERNING THIS APPLICATION AND THE LETTERS PATENT WHEN GRANTED SHOULD BE ADDRESSED TO THE UNDERSIGNED ATTORNEY OF RECORD.

Respectfully,

Michael E. Marion, Reg. 32,266
Attorney of Record

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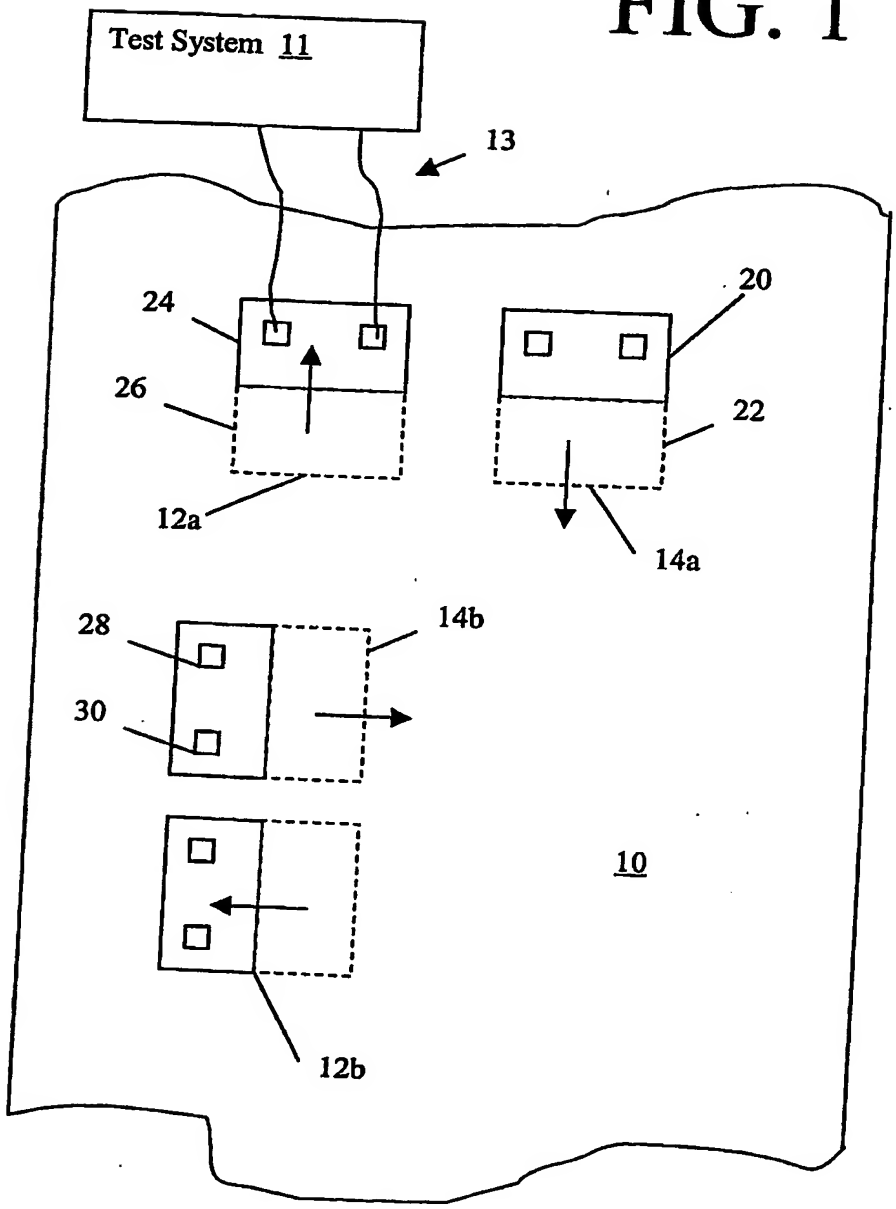
FIG. 1



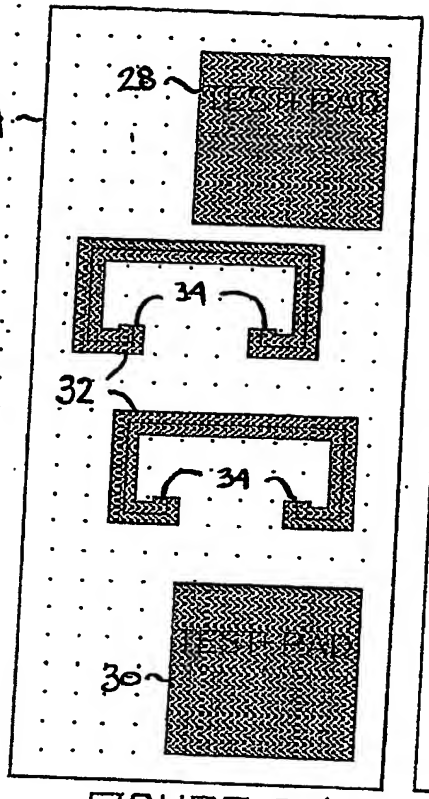


FIGURE 2A

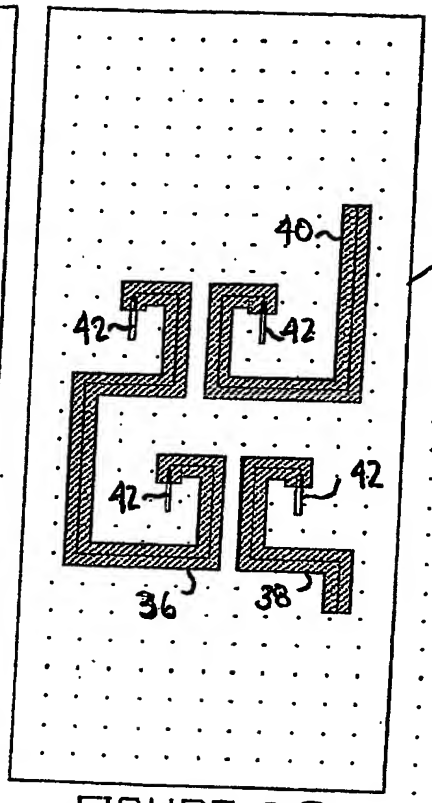


FIGURE 2B

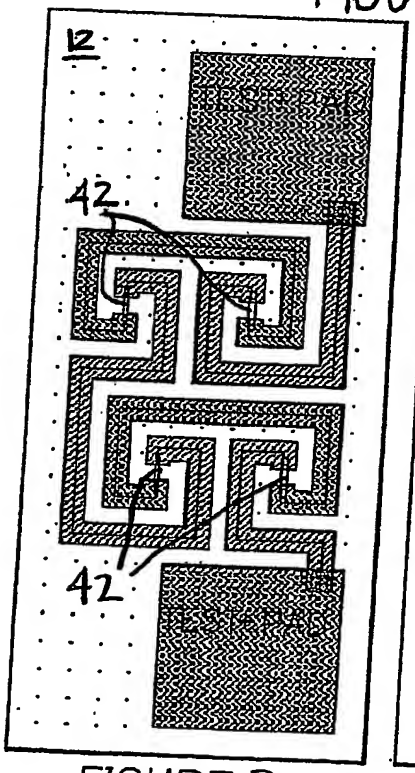


FIGURE 3

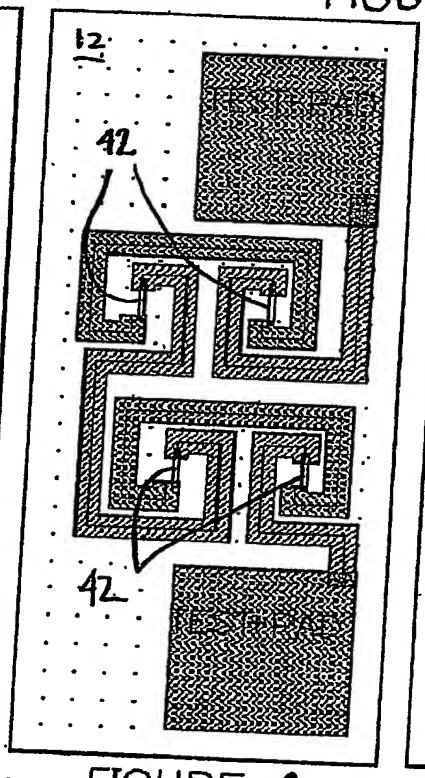


FIGURE 4

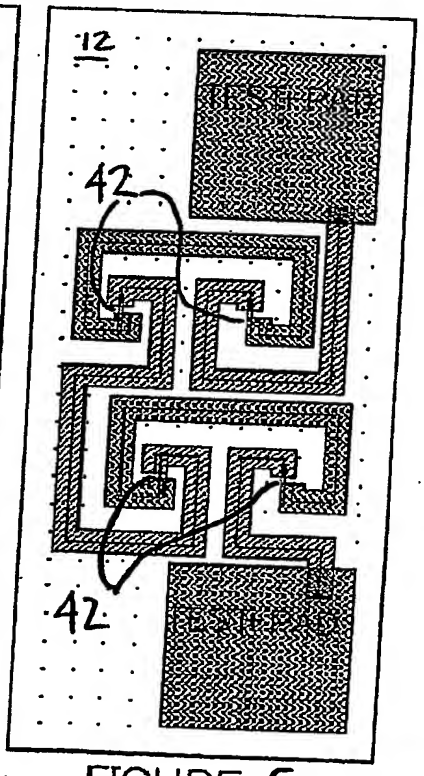


FIGURE 5

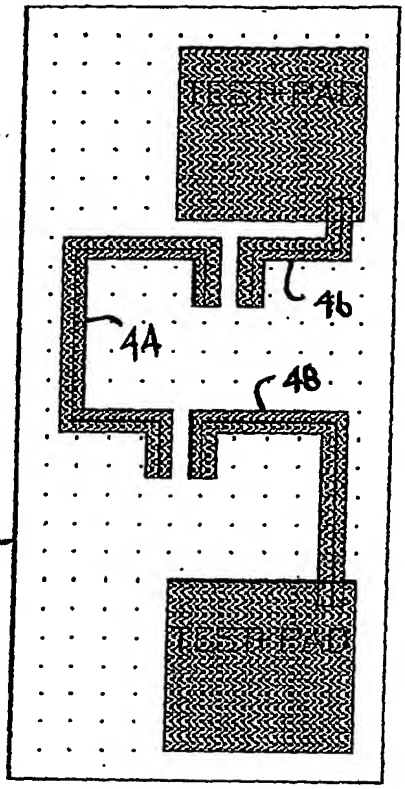


FIGURE 6A

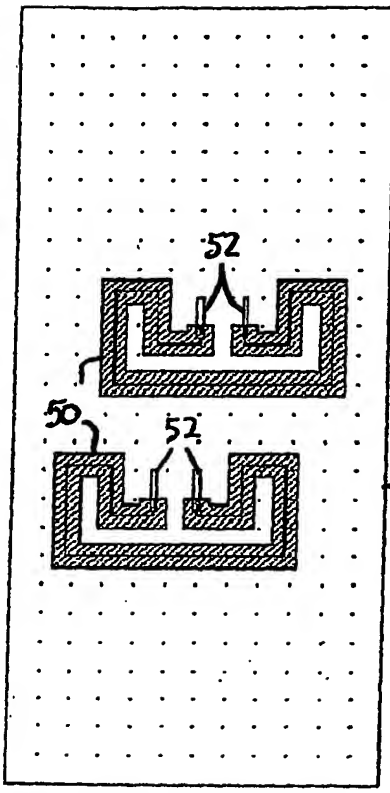
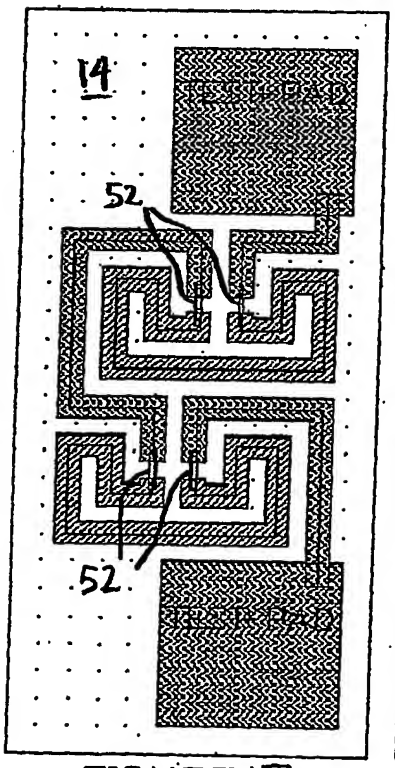


FIGURE 6B



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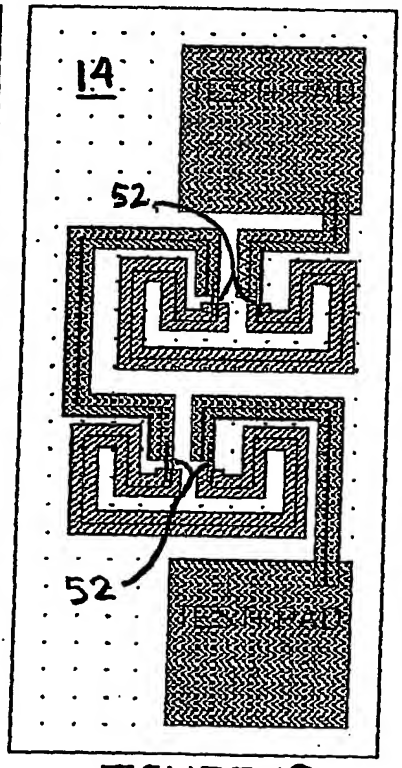

FIGURE 8

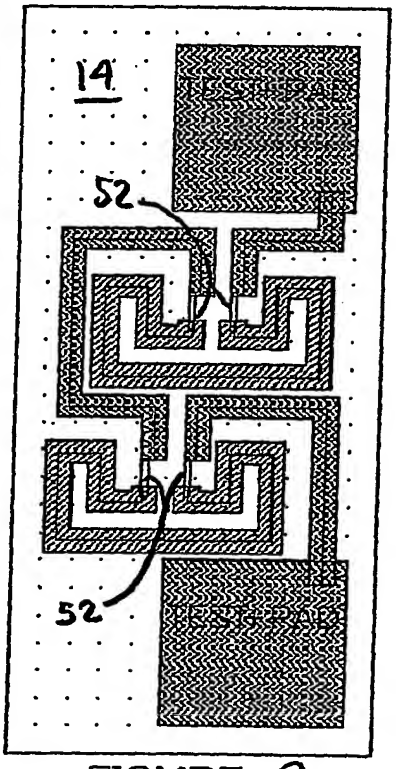

FIGURE 9

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